

WHAT IS CLAIMED IS:

1. An optoelectronic device, comprising:

2 a substrate having a first doped region adjacent a first outer
3 surface and a second doped region adjacent a second outer surface;
4 a wave guide located in said substrate and located between
5 said first outer surface and said second outer surface; and
6 a capacitor located over one of said first outer surface or
7 said second outer surface.

2 2. The optoelectronic device as recited in Claim 1 further
3 including a metal layer located on one of said first outer surface
4 or said second outer surface, said metal layer comprising a first
5 electrode of said capacitor, a dielectric located over said first
6 electrode and a second electrode located over said dielectric.

3 3. The optoelectronic device as recited in Claim 1 wherein
2 said optoelectronic device is a tunable laser and said substrate
3 further includes a gain region, a tuning region, an amplifier
4 region and a modulator region.

2 4. The optoelectronic device as recited in Claim 3 wherein
2 said substrate further includes a grating region.

5. The optoelectronic device as recited in Claim 3 wherein
2 said first doped region is a p-type doped region and said gain
3 region, said tuning region, said amplifier region and said
4 modulator region are located in said p-type doped region and said
5 second doped region is an n-type doped region and said capacitor is
6 located on said second outer surface and an electrode of said
7 capacitor is electrically coupled to said p-type doped region.

6. The optoelectronic device as recited in Claim 1 wherein
2 said substrate comprises indium phosphide and said first doped
3 region is a p-type doped region and said second doped region is an
4 n-type doped region and said capacitor is located on said second
5 outer surface.

7. The optoelectronic device as recited in Claim 1 wherein
2 a dielectric layer of said capacitor is a silicon dioxide or a
3 tantalum pentoxide.

8. A method of manufacturing an optoelectronic device,
2 comprising:

3 forming a first doped region adjacent a first outer surface of
4 a substrate;

5 forming a second doped region adjacent a second outer surface
6 of said substrate;

7 creating a waveguide in said substrate; and

8 forming a capacitor over one of said first outer surface or
9 said second outer surface.

10 9. The method as recited in Claim 8 wherein forming a
11 capacitor includes placing a first electrode metal layer on one of
12 said first outer surface or said second outer surface, forming a
13 dielectric over said first electrode and forming a second electrode
14 over said dielectric.

15 10. The method as recited in Claim 8 wherein said
16 optoelectronic device is a tunable laser and said method further
17 includes forming a gain region, a tuning region, an amplifier
18 region and a modulator region in said substrate.

19 11. The method as recited in Claim 10 further including
20 forming a grating region in said substrate.

12. The method as recited in Claim 10 wherein forming said
2 first doped region includes forming a p-type doped region and
3 forming said gain region, said tuning region, said amplifier region
4 and said modulator region includes forming said gain region, said
5 tuning region, said amplifier region and said modulator in said p-
6 type doped region;

7 forming said second doped region includes forming an n-type
8 doped region; and

9 forming said capacitor includes forming said capacitor on said
10 second outer surface and includes electrically connecting an
11 electrode of said capacitor to said p-type doped region.

12 13. The method as recited in Claim 8 wherein said substrate
13 comprises indium phosphide and forming said first doped region
14 including forming a p-type doped region and forming said second
15 doped region includes forming an n-type doped region and forming
16 said capacitor includes forming said capacitor on said second outer
17 surface.

18 14. The method as recited in Claim 8 wherein forming said
19 capacitor includes forming a dielectric layer comprising silicon
20 dioxide or tantalum pentoxide.

15. An integrated optoelectronic system, comprising:

at least one optical device, including:

an optical substrate having a first doped region adjacent a first outer surface and a second doped region adjacent a second outer surface;

a wave guide located in said substrate and located between said first outer surface and said second outer surface; and

a capacitor located over one of said first outer surface or said second outer surface;

an optical fiber coupled to said at least one optical device and located on or within said semiconductor substrate; and

a detector coupled to said at least one optical device.

16. The integrated optoelectronic system as recited in Claim 15 further including a metal layer located on one of said first outer surface or said second outer surface, said metal layer comprising a first electrode of said capacitor, a dielectric located over said first electrode and a second electrode located over said dielectric.

17. The integrated optoelectronic system as recited in Claim 15 wherein said optical device is a tunable laser and said optical substrate further includes a gain region, a tuning region, an

4 amplifier region and a modulator region.

18. The integrated optoelectronic system as recited in Claim
2 17 wherein said optical substrate further includes a grating
3 region.

19. The integrated optoelectronic system as recited in Claim
2 17 wherein said first doped region is a p-type doped region and
3 said gain region, said tuning region, said amplifier region and
4 said modulator region are located in said p-type doped region and
5 said second doped region is an n-type doped region and said
6 capacitor is located on said second outer surface and an electrode
7 of said capacitor is electrically coupled to said p-type doped
8 region.

20. The integrated optoelectronic system as recited in Claim
2 15 wherein said optical substrate comprises indium phosphide and
3 said first doped region is a p-type doped region and said second
4 doped region is an n-type doped region and said capacitor is
5 located on said second outer surface.